ePIC DAQ Status Update

Jeff Landgraf (BNL) for the ePIC Collaboration

Fernando Barbosa & Jeff Landgraf: Electronics & DAQ WG Conveners
Fernado Barbosa: WBS 6.10.08 (Electronics) CAM
Dave Abbott & Jeff Landgraf: WBS 6.10.09 (DAQ) CAMs

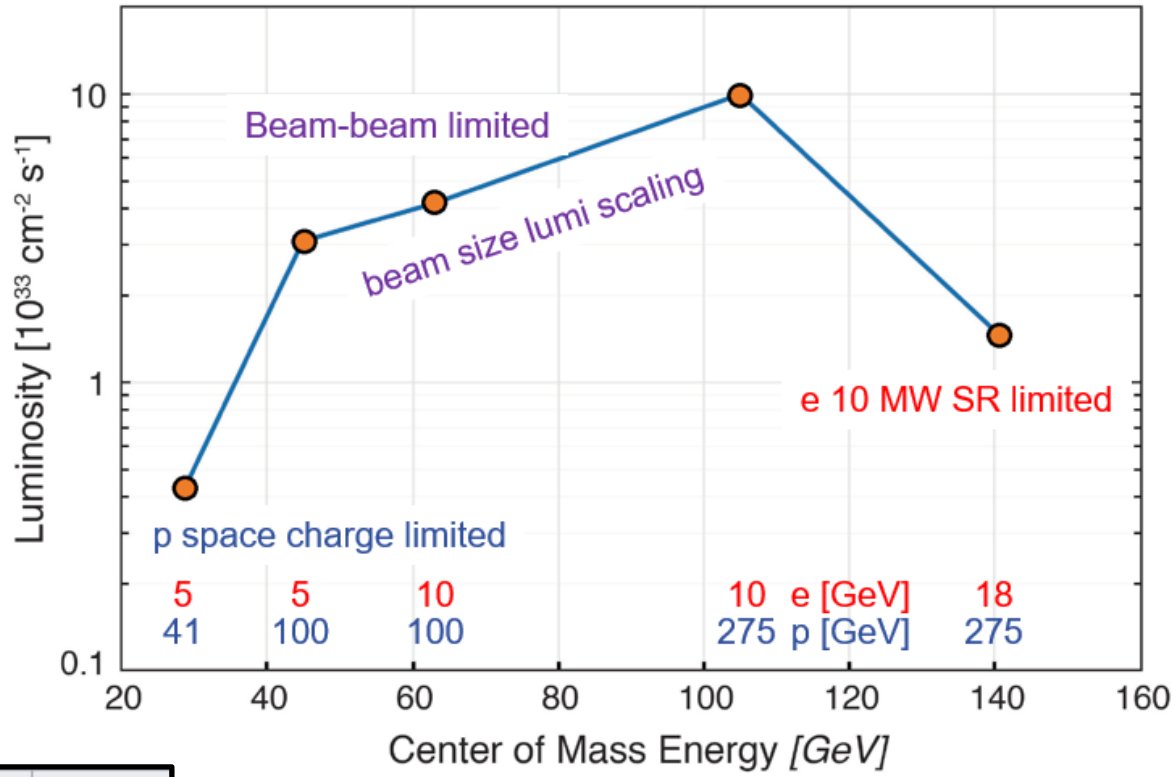
RHIC/AGS Users' Meeting
May 20, 2025
Electron-Ion Collider

Outline

- High level facts driving the requirements of the ePIC DAQ
- The streaming architecture of the ePIC DAQ
- Descriptions of the readout technologies
- Scale of the system and expected data flow
- Status of the components of the system

EIC Environment Impacts Detector Readout Requirements

- 1260 Bunches arriving at 98.5Mhz (10.15ns bunch separation)
  - Compare to 133 ns for light to transverse 40m
- 1.015us abort gaps (100 bunches)
- $\sqrt{s} \Rightarrow$ 20 – 141 GeV
- $\mathcal{L}_{max} \Rightarrow 10^{34}$ cm^{-2} s^{-1}
- Electron, proton, and light nuclei beams can be polarized.
  - DAQ must tag data to specific bunch crossings
  - Need to track luminosity for each bunch crossing



rates in kHz	5x41 GeV	5x100 GeV	10x100 GeV	10x275 GeV	18x275 GeV	Vacuum
Total ep	12.5 kHz	129 kHz	184 kHz	500 kHz	83 kHz	
hadron beam gas	12.2kHz	22.0kHz	31.9kHz	32.6kHz	22.5kHz	10000Ahr
	131.1kHz	236.4kHz	342.8kHz	350.3kHz	241.8kHz	100Ahr
electron beam gas	2181.97 kHz	2826.38 kHz	3177.25 kHz	3177.25 kHz	316.94 kHz	10000Ahr

ePIC Uses a Streaming DAQ and Computing

DAQ

Definition of streaming is “No L0 trigger”

- All data is zero suppressed by the front-end electronics
- No system wide deadtime in normal operation
- Collaboration should have the full ability to make data selection cuts on the widest possible criteria
  - Flexible event selection, data selection and background characterization
- But subject to an overall throughput budget of ~100Gb/sec

ePIC Streaming will include

- Capabilities for hardware and firmware-based triggering
- Capability for flow control
- Zero suppression & aggregation within data packets

Greater sensitivity to noise than triggered system

Greater sensitivity to backgrounds than triggered system

Computing

Definition of streaming is “Process data as it arrives”

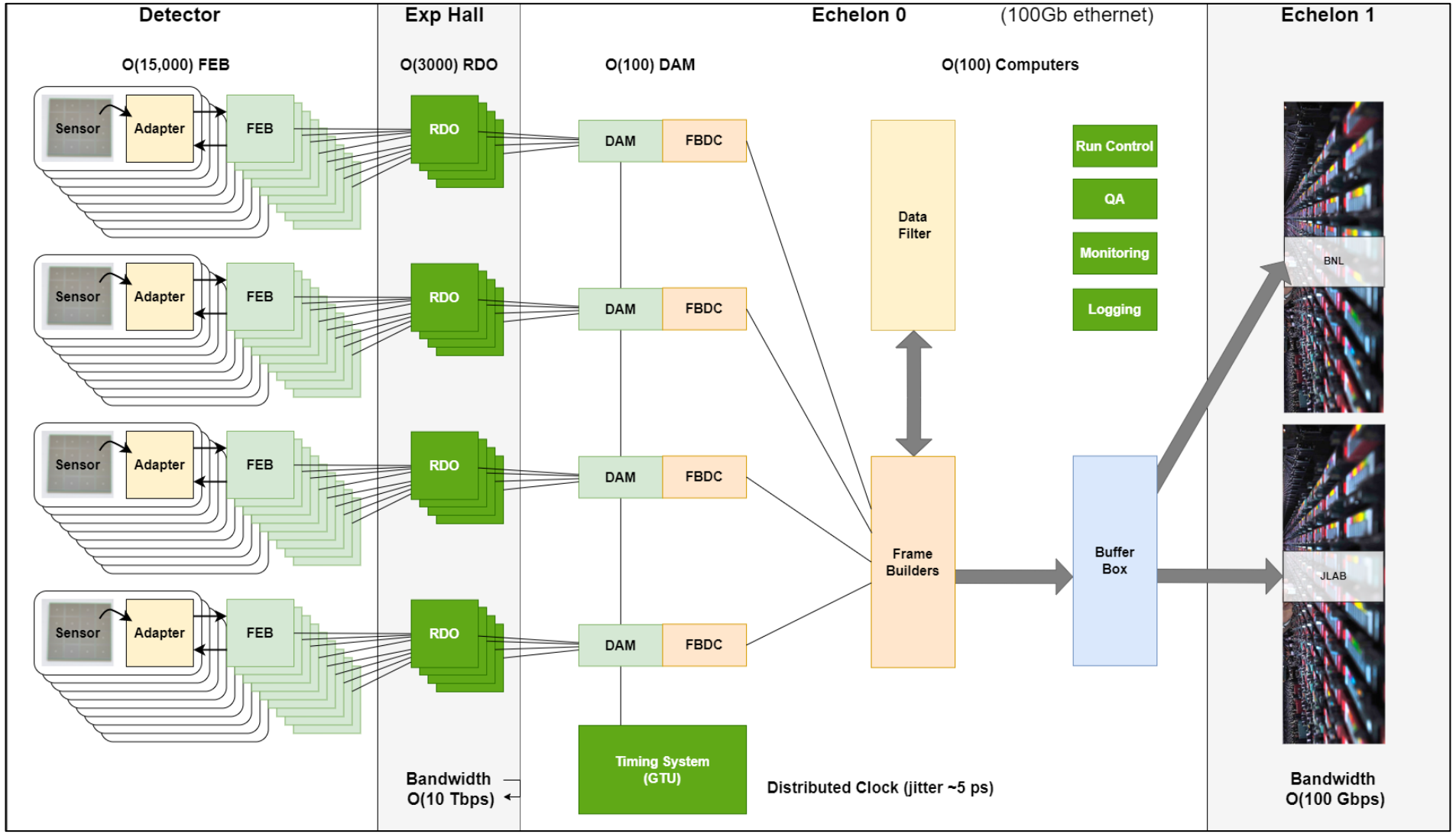
- Fast Analysis (~3 weeks not months or years) using automation of calibration and reconstruction.

Requires some overlap between DAQ/computing

- Automation of calibrations
  - Mapping calibration dependencies
  - Mapping application of calibrations
  - Mapping evolution of calibrations
- QA and monitoring can make use of full offline structure
- Consistent schemes and language for data/metadata
- Event selection / tagging / and accounting

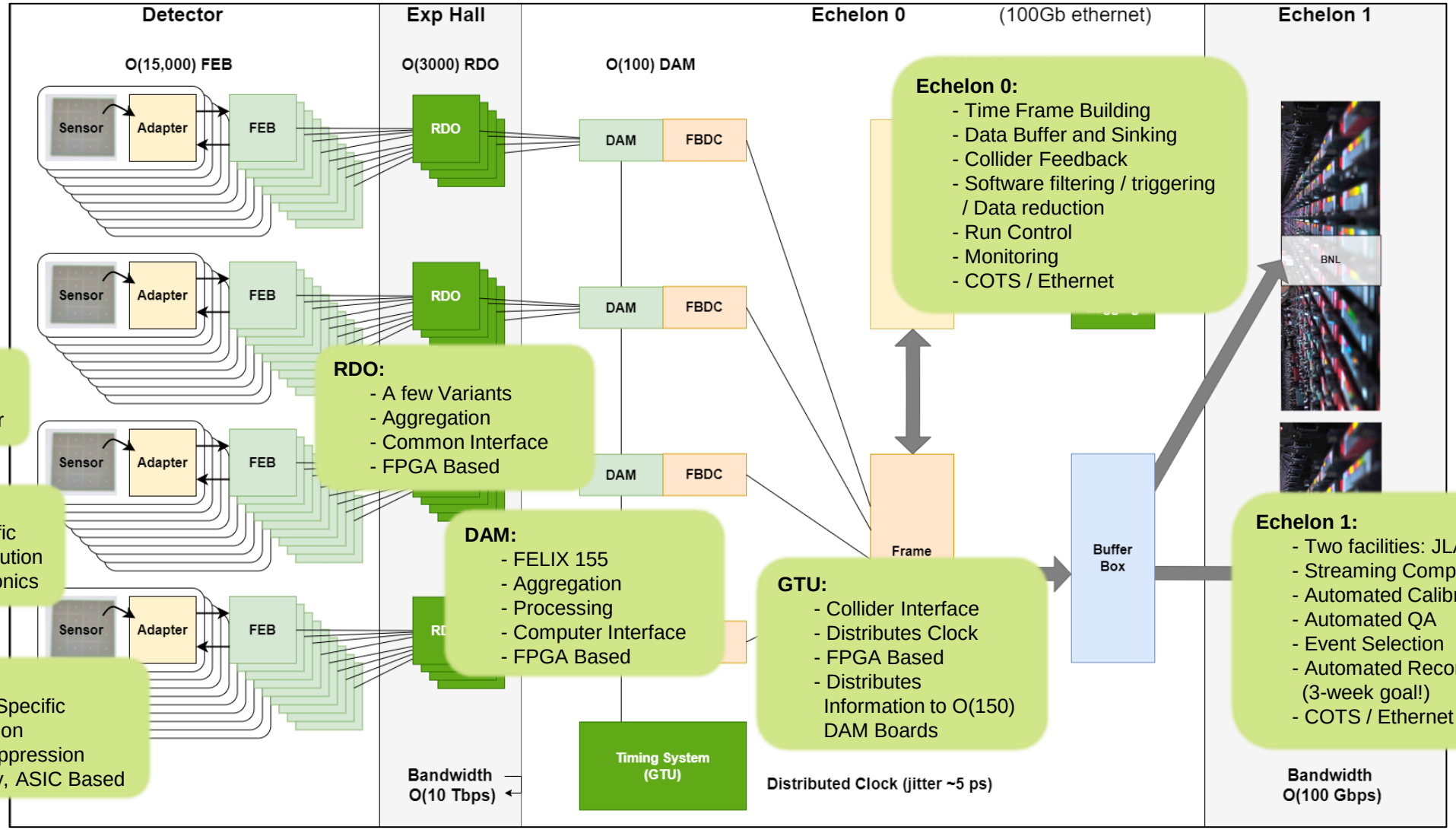
EIC Streaming DAQ/Computing Architecture

- Bunch Crossing
  ~10.2 ns/98.5 MHz
- Interaction Rate
  ~ 2 us/500 kHz
- Build Time Frames
  ~0.6ms



EIC Streaming DAQ/Computing Architecture

- Bunch Crossing ~10.2 ns/98.5 MHz
- Interaction Rate ~ 2 us/500 kHz
- Build Time Frames ~0.6ms



Sensor
- Detector Specific
- Multi-Channel Sensor

Adapter:
- Detector Specific
- HV/Bias Distribution
- Passive Electronics

FEB:
- Sensor Specific
- Digitization
- Zero Suppression
- Typically, ASIC Based

RDO:
- A few Variants
- Aggregation
- Common Interface
- FPGA Based

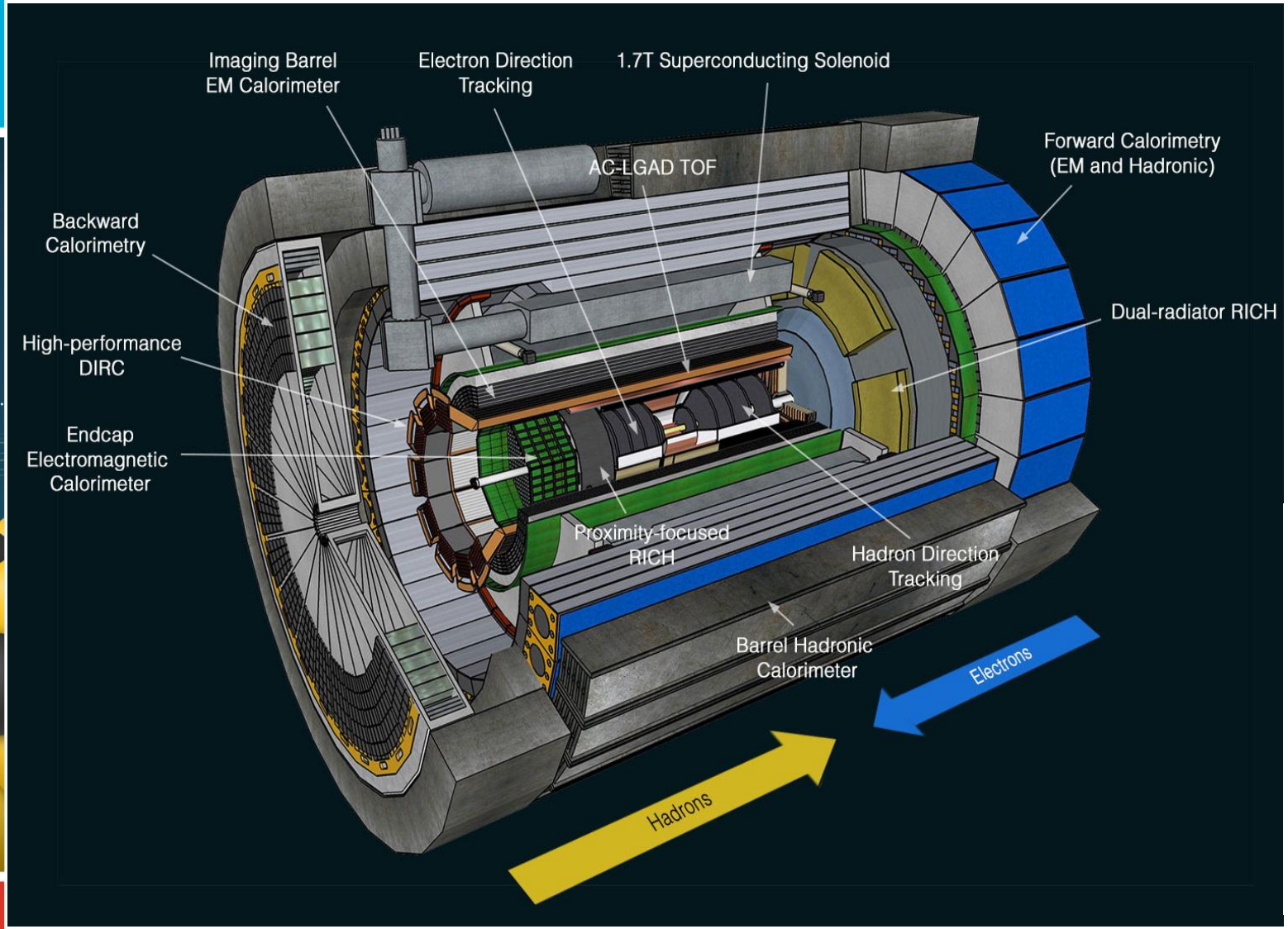
DAM:
- FELIX 155
- Aggregation
- Processing
- Computer Interface
- FPGA Based

GTU:
- Collider Interface
- Distributes Clock
- FPGA Based
- Distributes Information to O(150) DAM Boards

Echelon 0:
- Time Frame Building
- Data Buffer and Sinking
- Collider Feedback
- Software filtering / triggering / Data reduction
- Run Control
- Monitoring
- COTS / Ethernet

Echelon 1:
- Two facilities: JLAB/BNL
- Streaming Computing
- Automated Calibration
- Automated QA
- Event Selection
- Automated Reconstruction (3-week goal!)
- COTS / Ethernet

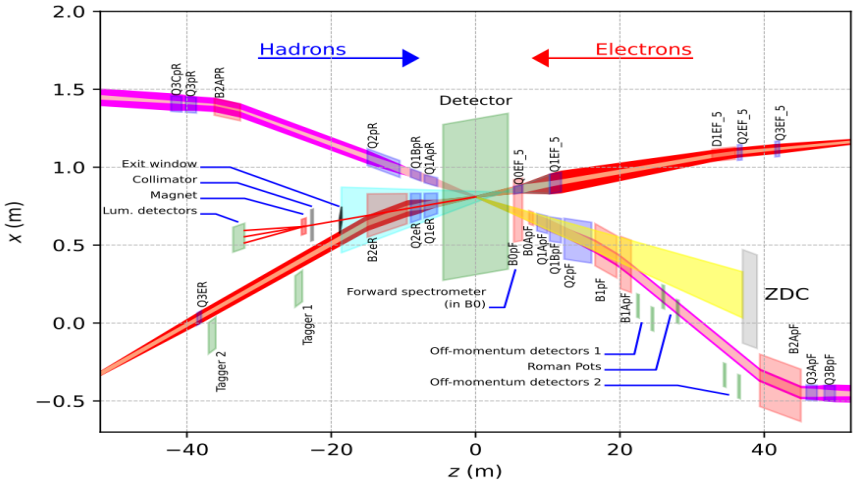
ePIC Readout Technologies



~30 Detectors

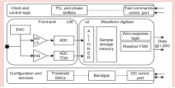
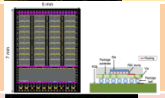
Spread over +/- 40 meters
(13 bunch crossings @ C)

Many technologies, but effort has been made to make use of possible synergy…



Front End Readouts & Synergies

ASIC Summary

Readout Technology	ASIC	Production	Institution	
Calorimeters, (14 Bit SiPM)	Discrete/COTS	FY27	Indiana University	
Calorimeters, (10-bit SiPM)	CALOROC	FY27	OMEGA / IN2P3 / IJCL, ORNL	
AC-LGAD, pixel	EICROC (32x32)	FY27	OMEGA / IN2P3 / IJCL / CEA-Irfu, AGH	
AC-LGAD, strip (HRPPD / MCP-PMT)	FCFD (128)	FY27	FNAL	
dRICH (SiPM, 1 p.e.)	ALCOR	FY26 – FY27	INFN	
MPGD	SALSA	FY27 – FY28	CEA-Saclay, U Sao Paulo	

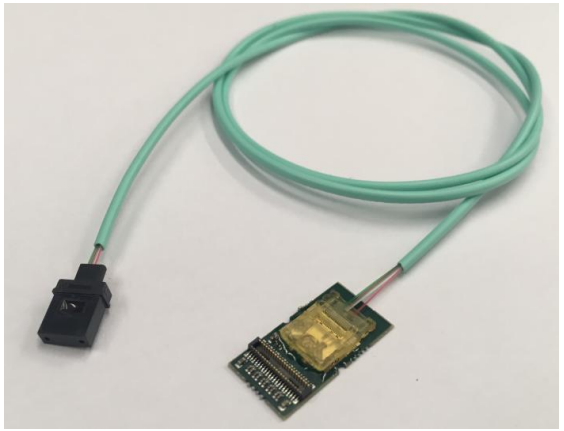
Versatile Link Plus Transceiver (VTRX+)

Inner Detector (SVT, dRICH, pfRICH, MPGDs, TOF, RP, B0, Offm)

- Radiation Tolerant
- Small Size / Mass
- Low Power

However,
- Final Fabrication Imminent
- No further (cost effective) production

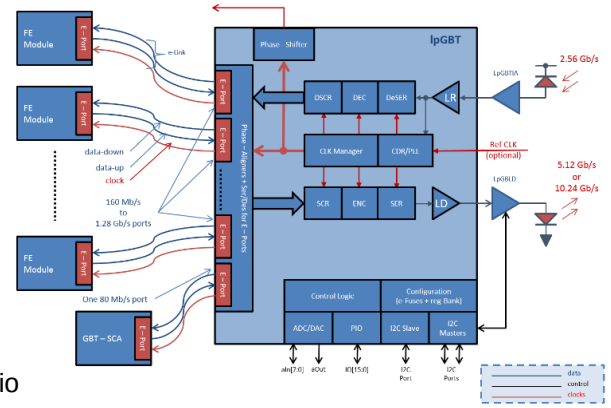
Final Design Review of VTRX+ and request part of CD-3B!



Low Power Giga Bit Transceiver (lpGBT)

- Aggregates and Serializes ASIC serial interfaces
- Radiation Tolerant
- Small Size / Mass
- Low Power
- Used with VTRX+ and possibly other optical transceivers

However,
- Runs at CERN clock (40MHz) rather than EIC clock (98.5 MHz)
- As do the ASICs originating from LHC
- ePIC DAQ requires multiple time references synchronized at 5:2 ratio



Characterization of DC/DC Converters

- Characterized CERN/Commercial products
- bPOL48V, bPOL12V
- Rad tolerant
- Magnetic Field tolerant

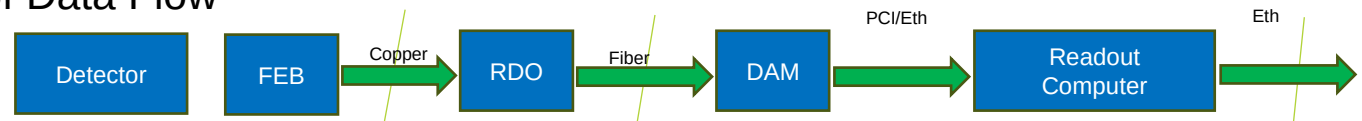

bPOL48V w/ bottom mount heat-sink, 300nH @ 1.5MHz
Inductor dimensions: 10 x 12.0 x 7.5mm (LxWxH)


bPOL12V NO heat-sink, 220nH @ 2.0 MHz
Inductor dimensions: 10.3 x 6.5 x 3.5mm

Summary of Channel Counts and Data Flow

Detector Group	Channels					Det Fiber Down	Det Fiber Up	RDO	Fiber Pair (DAQ)	DAM	Data Volume (RDO) (Gb/s)	Data Volume (To Tape) (Gb/s)
	MAPS	AC-LGAD	SiPM/PMT	MPGD	HRPPD/ MCP-PMT							
Tracking (MAPS)	16B					183	5863	183	183	7	15	15
Tracking (MPGD)				164k		640	2560	160	160	5	27	5
Calorimeters	500M		100k					522	522	17	70	17
PID (TOF)		6.1M				500	1364	500	500	14	50	12
PID Cherenkov			318k		143k			1283	1283	32	1275	32
Far Forward		1.5M	10k					80	80	6	36	12
Far Backward	66M		0.5k					25	289	11	37	8
Lumi		128k	3.5k					41	41	4	264	8
Polarimetry	Independent Electronics, DAQ, & Controls from central detector but expected to build on same technologies											
TOTAL	**16.6B**	**7.7M**	**432k**	**164k**	**143k**	**843**	**9,787**	**2,794**	**3,058**	**95**	**1,774**	**109**

Summary of Data Flow



Aggregate	2.0 Tb/sec
Noise	1.6 Tb /sec
Signal from Physics + Background	400 Gb / sec

Aggregate	2.0 Tb/sec
Per RDO (Avg)	0.7 Gb/sec

Aggregate	109 Gb/sec
Collision Signal	62 Gb/sec
Synchrotron Rad	Under design
Electron Beam	4.5 Gb/sec
Hadron Beam	1.0 Gb/sec
Noise	41 Gb/sec

Scale of the system:

- Electronics
  - ~ 30 detectors
  - ~ 5 Readout Technologies
  - ~ 3000 RDOs (on detector/in racks)
  - ~ 100 DAM boards (DAQ room)
  - GTU (with interface boards)
- Maximum Data Volume
  - ~ 2 Tb/sec digitized
  - ~ 100Gb/sec recorded

System Components Status

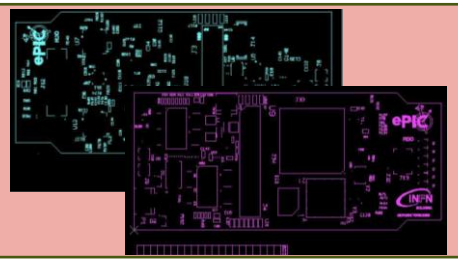
RDO

FPGA/SFP+

- TOF Pre-prototype was used for timing studies
- TOF moved to lpGBT (direct to DAM)
- To be picked up for Calorimeters

FPGA/VTRX+

- INFN Bologna for dRICH
- 12 Populated PCBs expected June
- FPGA: Artix Ultrascale+ Class



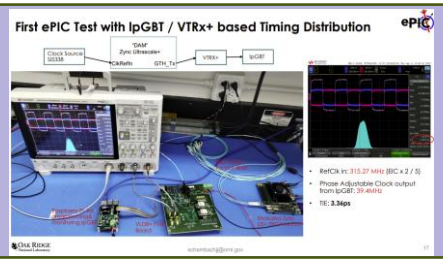
Fiber Aggregation (MAPS)

- (ITS3/AC-LGAD/others)
- Component Counts

GTU

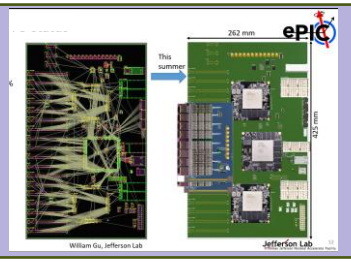
Reconstructed Clock Timing Tests:

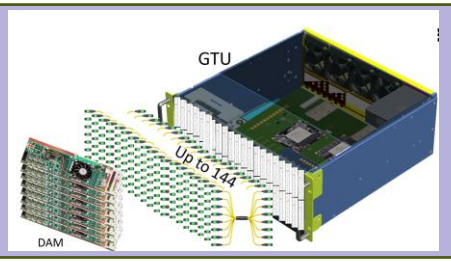
- Mocked up with dev-kits
- < 5ps timing measured with Ultracale+ FPGA and with lpGBT/VTRX+



Electronics Design:

- Schematics 60%
- PCB placement 80%
- PCB routing 0%
- William Gu





DAM

FLX-182

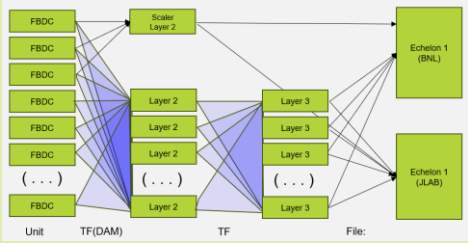
- Developed by ATLAS (Omega Group at BNL)
- 2 FELIX engineering articles obtained

FLX-155

- Targeted for ePIC use
- Undergoing testing in Omega Group
- Test articles 2025

Echelon 0 Compute

- Readout Computers
- Frame Building Computers
- Data Reduction
  - Filters
  - Compression
  - High Level Filtering
- DAQ Logging
- DAQ Monitoring
- DAQ QA
- Configuration
- Slow Controls interface (IOC)
- Buffering and Data Transfer
- 40 MHz / 100 MHz clocks by DAM
- Time Frames up to 2^16 BX long (.6 ms)
- Data Formats
- Construction of Time Frames and Super Time Frames
- Run Control Model



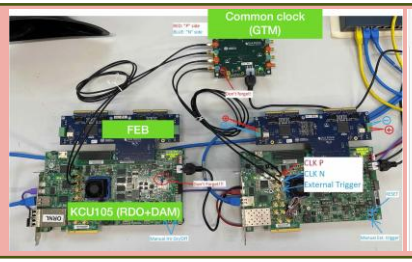
System Components Status

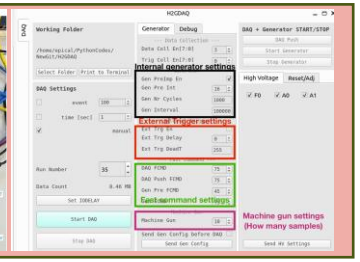
picoDAQ

Jan 2026
- First of O(Yearly) DAQ releases
- Select / Merge / Document useful features from existing systems
- Test stands tend to merge RDO/DAM (little aggregation)

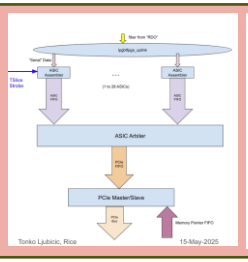
Currently defining picoDAQ
- Goal is reading out test stands:
- Provide common services
- Support common hardware
- Develop towards final DAQ
- Not expected to be turnkey!

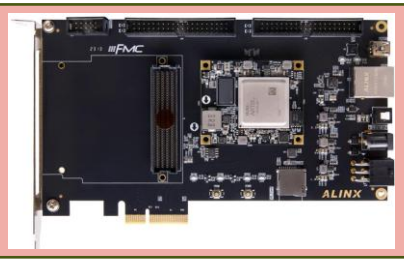
BHCAL --- (H2GCROC)
- KCU105 (RDO+DAM) (kintex)
- Python Config/Control
- rcdaq integration
- Norbert Novitzky, Miklos Czeller, Gabor Nagy, Shihai Jia, Martin Purschke



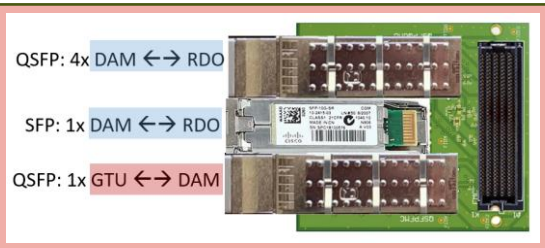


TOF DAM-Lite: (ETROC)
- Alinx AXAU15 (artix)
- Reads from lpGBT
- ~Follows FELIX development scheme
- Tonko Ljubicic





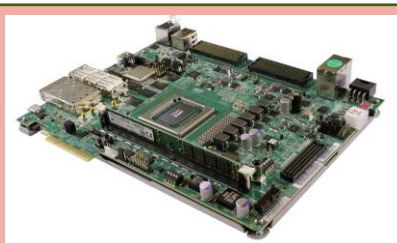
FMC - Q(SFP) Adapter
- Allows use of prototype GTU with dev boards (such as AXAU15)
- 4-Boards (June)
- William Gu



Firmware Support for Commercial Development Boards planned as FELIX substitutes for test stands (to be developed)

2 Port VD100 (versal) ($800)

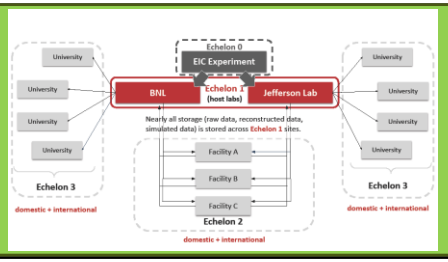
48 port VMK180 (versal) ($10k)



Echelon 1 Compute Interface

Streaming Readout Working Group
- Requirements for Data TX
- Test Beds to be developed
  - TX / Data management (e.g. Rucio)
  - Orchestration / State Model (e.g. Panda)
  - Streaming Reconstruction (JANA2)
  - Calibration workflows

Interface:
- Full Data to be streamed to JLAB/BNL echelon 1
- Full Data to be archived at both facilities for redundancy



Use Case	Echelon 0	Echelon 1	Echelon 2	Echelon 3
Streaming Data Storage and Monitoring	✓	✓		
Alignment and Calibration		✓	✓	
Prompt Reconstruction		✓		
First Full Reconstruction		✓	✓	
Reprocessing		✓	✓	
Simulation		✓	✓	
Physics Analysis		✓	✓	✓
AI Modeling and Digital Twin		✓	✓	

Summary

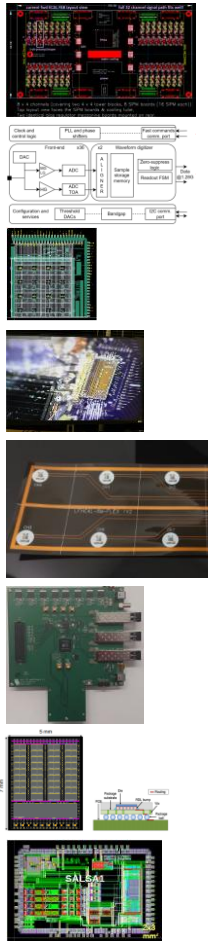
- Described an overview of the readout system for ePIC
- Described the expected data volumes expected from noise, background and collisions.
- Defined the current status of Electronics and DAQ Components

Questions?

Back-up

ASICs & Electronics – Component Status

	Readout Technology	Status & Development Summary	Production	Institution
Discrete/COTS	Calorimeters, SiPM, 14-bit	Devices selected, PCB design practically completed. Beam tests FY24-FY25, Eng. Article FY26	FY27	Indiana University
CALOROC	Calorimeters, SiPM, 10-bit	Interface design FY23- FY24, CALOROC1A/B designed FY24-FY25, CALOROC2 (64 ch) FY25-FY26	FY27	OMEGA/IN2P3/IJCL, ORNL
EICROC (32x32)	AC-LGAD, pixel	EICROC0A (4x4) designed FY24-FY25, EICROC1 (8x32) FY25, EICROC2 (32x32) FY26	FY27	OMEGA/IN2P3/IJCL/CEA-Irfu, AGH
FCFD (128)	AC-LGAD, strip	Front end characterized, FCFDv1 (6 ch) FY23-FY24 characterized, FCFDv2 FY25-FY26	FY27	FNAL
Low-Mass Hybrid	AC-LGAD TOF	Pre-prototypes fabricated and co-cured onto Barrel TOF stave prototypes. Develop low cost hybridization techniques FY25-FY26	-	ORNL
High Precision Clock Distribution	AC-LGAD, all	ppRDO PCB (6) complete, Jitter = 3 ps. Finalize development for TOFs, FF, FB detectors with use of EICROC and FCFD ASICs in FY25-FY26	-	BNL/LBNL/RICE
ALCOR	dRICH, SiPM, 1 p.e.	ALCORv2.1 (32 ch) beam tests FY24, ALCOR v3 (64 ch) FY24-FY26	FY26 – FY27	INFN
SALSA	MPGD	SALSA0/1 FY24, SALSA2 (32 ch) designed FY23-FY25, SALSA3 (64 ch) FY25-FY26	FY27 – FY28	CEA-Saclay, U Sao Paulo



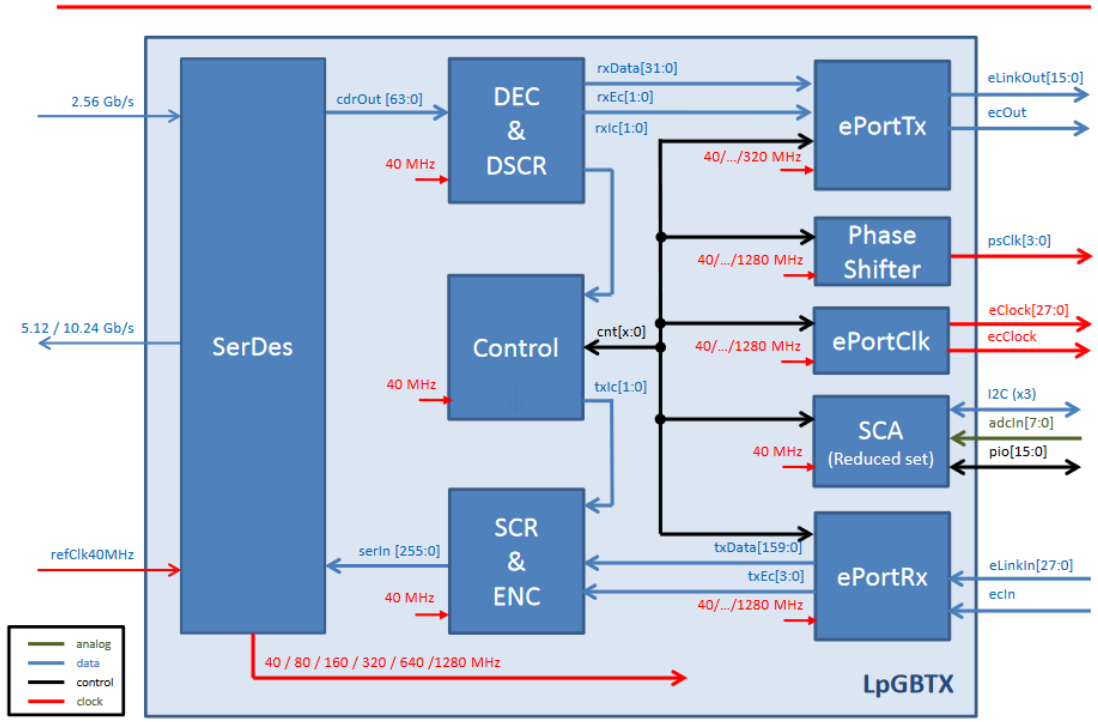
- ASIC production is ~1 Year: Fab, Packaging, Test. Additional information is included in the Backup slides.

Complete. Fab submission is imminent.

lpGBT – Low Power Giga-bit Transceiver

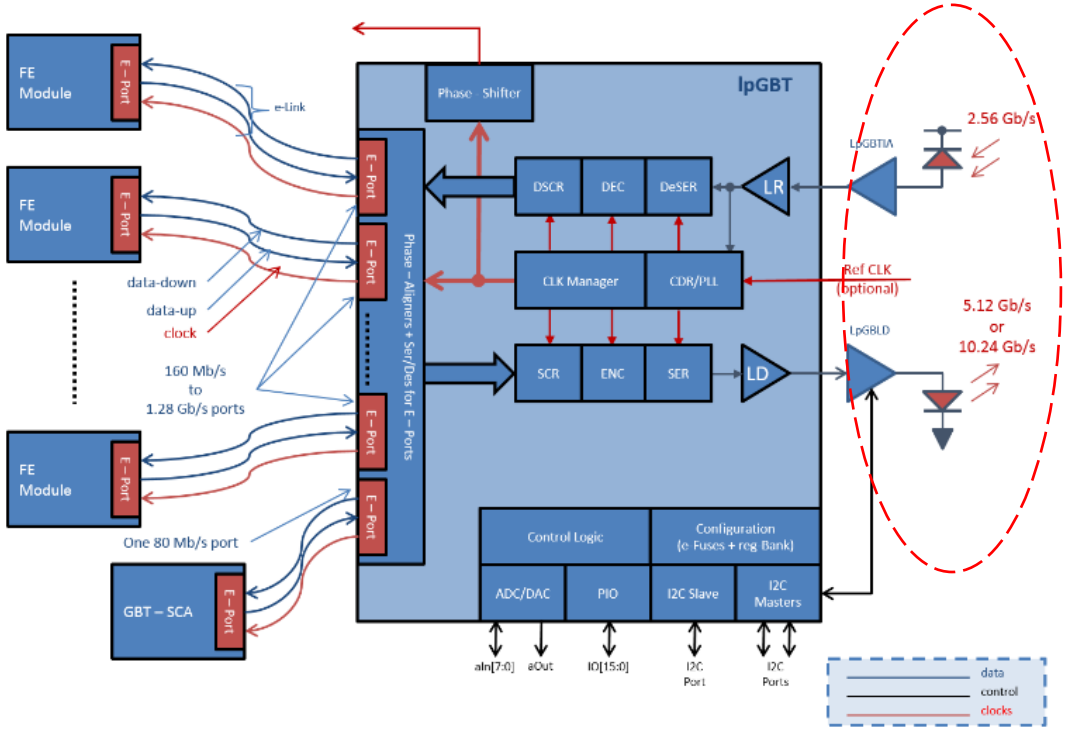
Charge 1, 2, 7

LpGBTX Block Diagram



Application

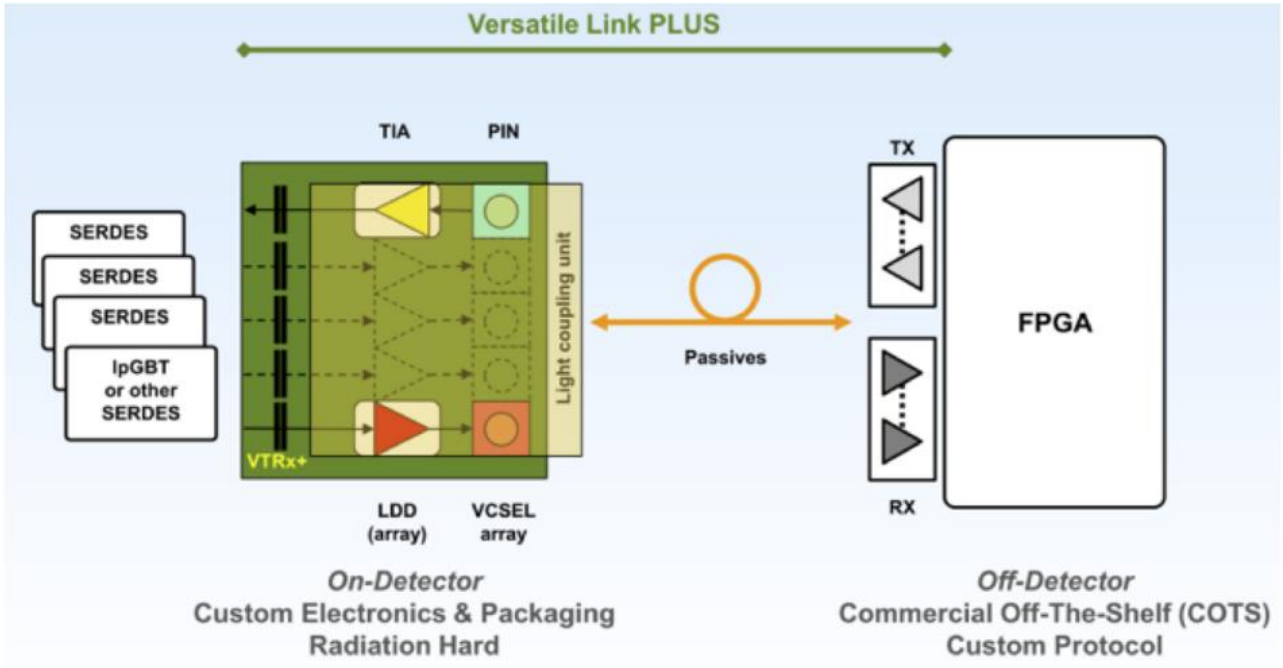
Replaced with VTRX+

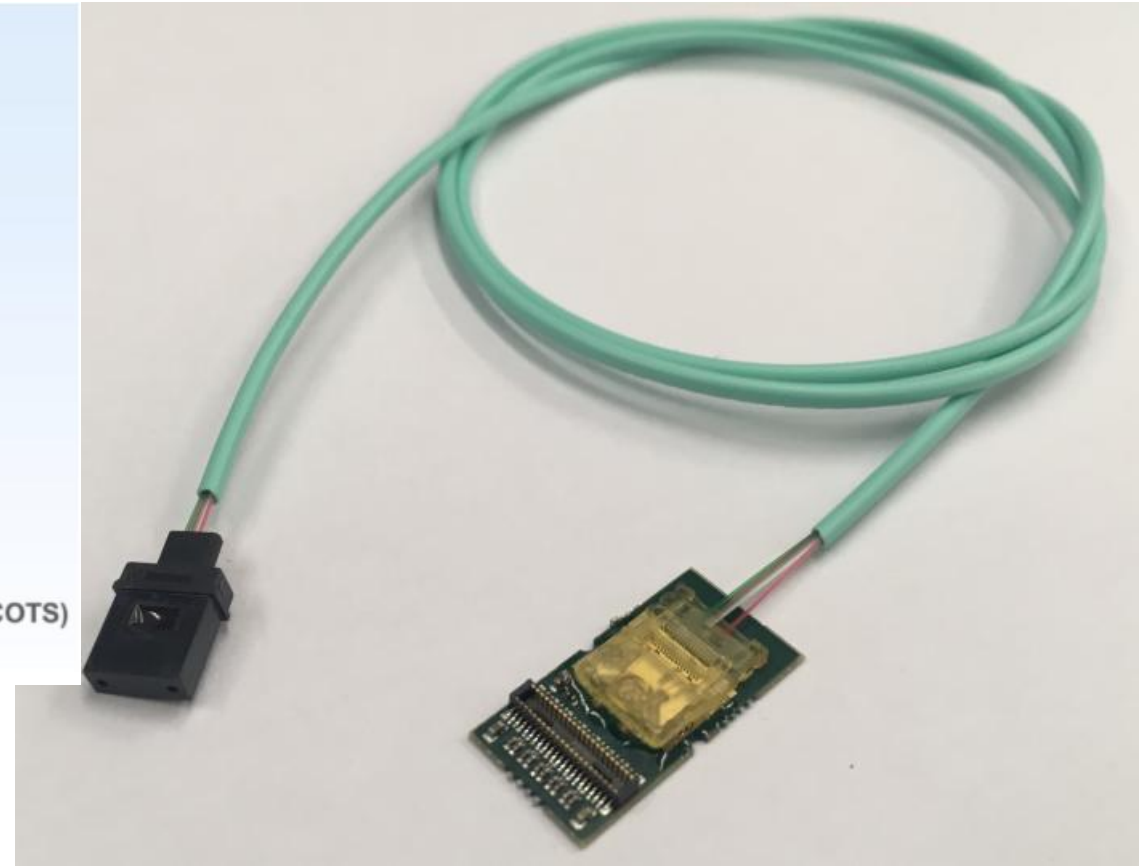


- Operation up to 12.24 Gbps Input [Up-link, elink up to 1.28 Gbps], and up to 2.56 Gbps Output [Down-link, elink up to 320 Mbps].
- Power consumption up to 750 mW.
- Radiation hardness to 200 Mrad TID, SEU robust.
- BGA, 9 mm x 9 mm x1.24 mm.

VTRX+ – Versatile Link+ Transceiver

Charge 1, 2, 7





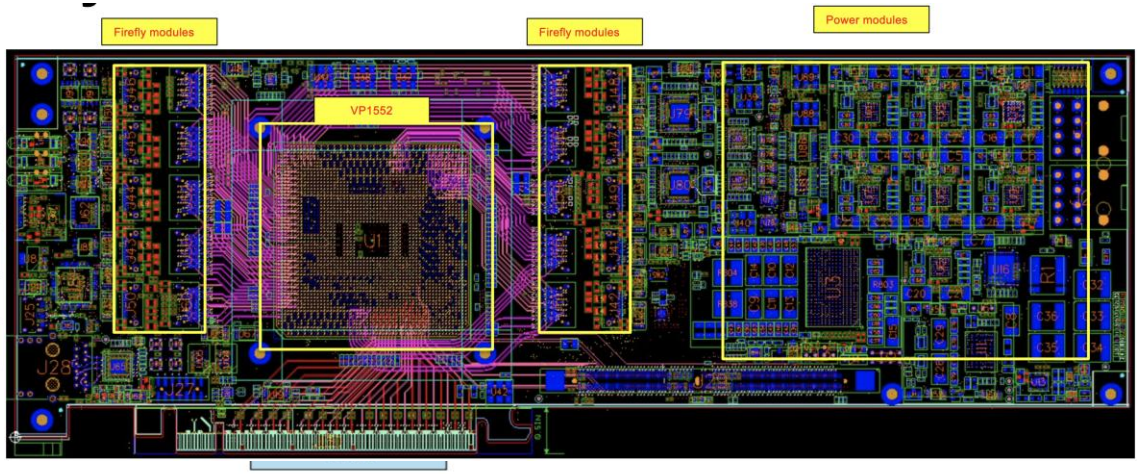
- Tx Data rate up to 10.24 Gbps.
- Rx Data rate up to 5.12 Gbps.
- Power consumption up to 320 mW.
- Fiber pigtail length [200 mm to 1000 mm], to be specified by customer. Low Smoke Halogen-Free Polymer.
- Radiation Hard.
- Magnetic field up to 4 T.

FELIX Updates – FLX-155

Charge 3

- FELIX (Front-End Link Exchange) hardware for future ATLAS experiments at HL-LHC is being developed at BNL (Omega Group)
  - Long term support is insured. Development timelines are compatible with EIC.
  - ePIC is collaborating with Omega to use this design as our DAM board.
- Latest (FLX-155) design review completed by ATLAS and AMD
  - It has been sent out for fabrication. PCBs available by July.
- First 4 populated boards expected by late August/early September
  - We expect to receive at least one board by the end of this year

- Versal Premium: XCVP1552-VSVA3340
- Support PCIe Gen4 x16, 2 Gen5 x8
- 48 FireFly data links (10/25 Gb/s)
- 4 LTI links (10/25 Gb/s)
- 100GbE (4*25Gb/s)
- DDR4
- GbE
- White Rabbit
- Electrical IOs (single-ended)



Note: 4 fiber LTI Link supports receiving either reconstructed or a direct clock

Versal FPGA is a SoC (Dual Core ARM) and can operate either standalone or in a Server

EPIC Detector Scale and Technology Summary:

6/6/2024

Detector System		Channels	RDO	Gb/s (RDO)	Gb/s (Tape)	DAM Boards	Readout Technology	Notes
Si Tracking:	Inner Barrel (IB)	1.8B Pixels	24	2.36	2.36	1	ITS-3 sensors &	RDO corresponds to number Slow Controls lpGBT.
	Outer Barrel (OB)	5.0B Pixels	55	3.52	3.52	2	ITS-2 staves / w improvements	(~ 36 simplex fibers / RDO)
	Backward Disks (EE)	4.7B Pixels	52	4.68	4.68	2		
	Forward Disks (HE)	4.7B Pixels	52	4.68	4.68	2		
MPGD tracking:	Electron Endcap	16,384	16	2.86	0.58	1	uRWELL / SALSA	SALSA:
	Hadron Endcap	16,384	16	4.01	0.80	1	uRWELL / SALSA	64 Ch/Salsa
	Inner Barrel	32,768	32	4.10	0.82	1	MicroMegas / SALSA	4 Salsa/FEB
	Outer Barrel	98,304	96	15.81	3.16	2	uRWELL / SALSA	4 FEB / RDO
Forward Calorimeters:	LFHCAL	63,280	74	18.54	2.47	2	SiPM / CALOROC	CALOROC:
	HCAL insert	8k	9	17.72	2.36	1	SiPM / CALOROC	56 Ch/CALOROC
	ECAL W/SciFi	16,000	64	14.75	7.36	2	SiPM / Discrete	16 CALOROC / RDO
Barrel Calorimeters:	HCAL	1,536	2	0.87	0.12	1	SiPM / CALOROC	
	ECAL SciFi/PB	5,760	4	11.45	1.52	1	SiPM / CALOROC	Discrete:
	ECAL ASTROPIX	500M pixels	340	1.25	1.25	8	Astropix	32 Ch/FEB,
Backward Calorimeters:	NHCAL	3,256	4	3.46	0.47	1	SiPM / CALOROC	8 FEB/RDO conservative (16 estimate).
	ECAL (PWO)	2,852	13	2.00	0.99	1	SiPM / Discrete	
Far Forward:	B0: Crystal Calorimeter	135	1	2.3	2.3	1	SiPM/APD / Discrete	
	4 AC-LGAD layer	688,128	30	12.75	2.1	1	AC-LGAD / EICROC	4 layer x 42 module x 4 EICROC x 1024 ch
	2 Roman Pots	524,288	22	14.53	2.1	2	AC-LGAD / EICROC	2 stations x 2 layer x 32 module x 4 EICROC x 1024 ch
	2 Off Momentum	292,912	12	3.53	0.7	1	AC-LGAD / EICROC	2 stations x 2 layer x 18 module x 4 EICROC x 1024 ch
	ZDC: Crystal Calorimeter	900	4	2.30	4.5	1	SiPM/APD / Discrete	
	HCAL	9,216	11	0.22	.22	1	CALOROC	
	Imaging low-gran*	60,480	68			2	CALOROC	In-kind Japan (not in baseline)
	Imaging hi-gran*	100,980	112			3	CALOROC	In-kind Japan (not in baseline)
	Veto*	33,660	38			1	CALOROC	In-kind Japan (not in baseline)
Far Backward:	2 x Low Q Tagger	66M pixels	24	37	.3	10	Timepix4	Firmware Trigger to reduce output rate
	2 x Low Q Tagger Cal	420	1	-	-	1	SiPM / CALOROC	Low Q Calorimeter doesn't run at high luminosity
	2 x Lumi PS Calorimeter	3,360	1	19	7	1	SiPM / Discrete	
	2 x Lumi PS tracker	128k	10	45	2	1	AC-LGAD: FCFD or EICROCx	
	Direct Photon Lumi Cal	100	24*	200	7	1	SiPM / fADC250	Direct Photon: commercial digitizer, no RDO
PID-TOF:	Barrel	2,359,296	288	15.95	4.79	8	AC-LGAD: FCFD or EICROCx	bTOF 128 ch/ASIC, 64 ASIC/RDO
	Endcap	3,719,168	212	33.92	7.34	6	AC-LGAD: EICROC	eTOF 1024 pixel/ASIC, 24-48 ASIC/RDO (41 ave)
PID-Cherenkov:	dRICH	317,952	1242	1240	13.5	30	SiPM / ALCOR	Worse case after radiation. Includes 30% timing window. Requires further data volume reduction
	pfRICH	69,632	17	24	12.5	1	HRPPD / FCFD or EICROCx	Firmware trigger
	DIRC	73,728	24	11	6	1	MCP-PMT / FCFD or EICROCx	

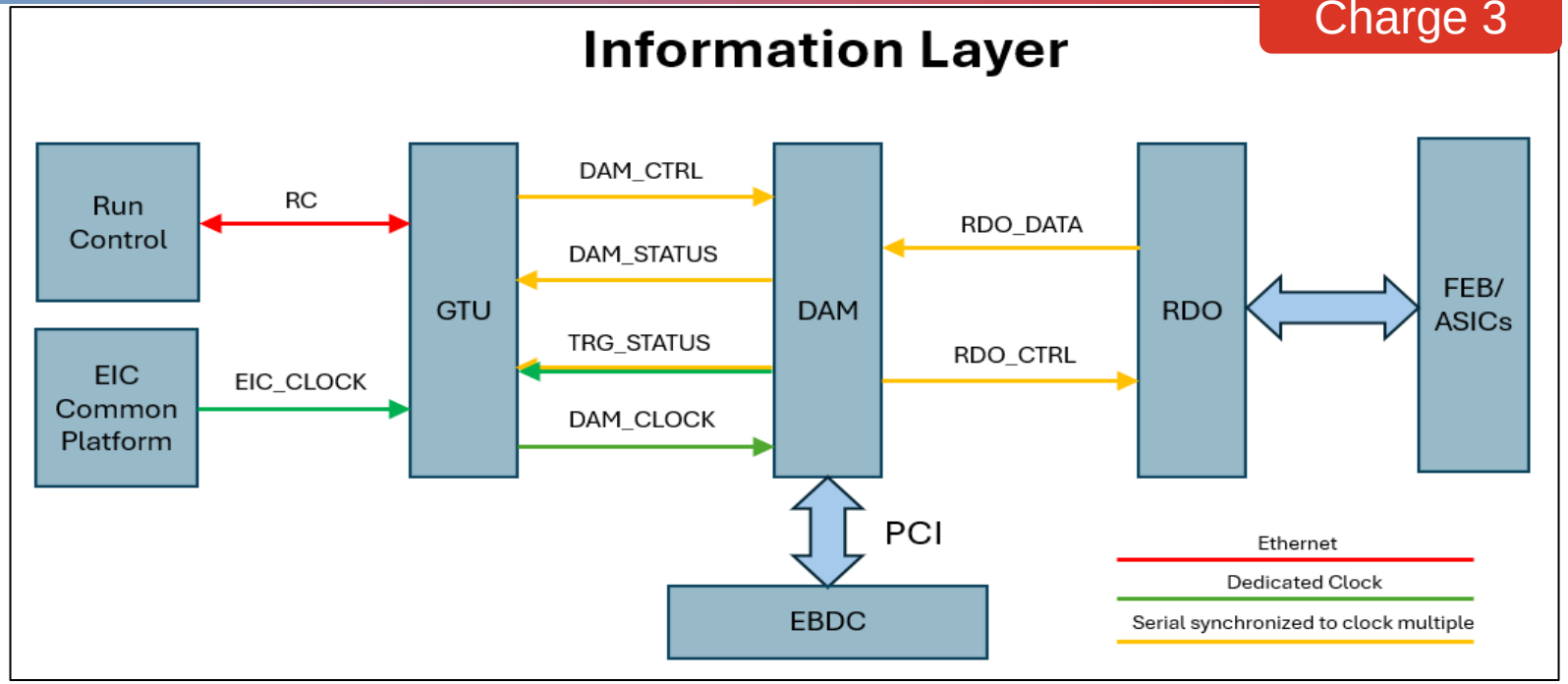
Fiber Protocol / DAQ operation

Charge 3

Synchronous Commands:

64 bits (80 bits 8b/10b encoded) per bunch

- Reconstructed clock
- Redundant BCO
- Distinct synchronous commands (eg)
  - RC
  - Time Frame Control & Definition
  - Flow Control
  - Trigger
    - Request special events
    - Data filter (firmware trigger)
  - Configuration (ASIC / RDO firmware)
  - Data Formatting
  - Data Transfer
    - Hits
    - Slow Controls



Trigger Operation:

- Support Max Data Volume to DAM / Readout computer Buffers
- Generate Trigger Signals in DAM
- Communicate triggered crossings via synchronous cmds through GTU

Time Frame Definition:

- 16 bits BCO (0.66ms -> 8MB @ 100Gbps)
- Flexible formatting
  - Filtered & Unfiltered data can coexist
- Time Frames are built, they contain the full set of detectors for the time period
- Tiered Data Format.
  - High level flexible, named navigation via banks (e.g. star SFS, sPHENIX DAQRC)
  - Low level supports direct, detector specific (eg ASIC) formats.

Slow Controls Status

Charge 1&3

- Slow Controls Components and architecture are identified

- EPICs Base
  - Allows use of existing tools
  - Synergy with EIC Controls